REMARKS

The above amendments and these remarks are in reply to the Advisory Action mailed on October 10, 2001 and the Final Office Action dated July 18, 2001. Claims 1-2, 8-10 and 16-17 are now pending. Claims 16 and 17 have been rejected under 35 U.S.C. §112 as containing subject matter which was not described in the specification. Claims 1 and 16 have been rejected under 35 U.S.C. §102(b) as being anticipated by Middelhoek et al.(U.S. Patent Number 5,216,269). Claims 8 and 10 have been rejected under 35 U.S.C. §102(e) as being anticipated by Chang et al.(U.S. Patent Number 6,126,060). Claims 2 and 17 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Middelhoek et al. in view of Chang et al. Claim 9 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Chang et al. in view of Middelhoek et al. Applicants respectfully traverse each of the rejections as explained below. Claims 1, 8 and 16 have been amended in order to overcome the rejections as explained below. Support for amended claims 1, 8 and 16 is found in the specification of the originally filed application. No new subject matter has been added. Applicants thank the Examiner for careful review of the claims. Applicants further thank the Examiner for the interview granted on October 15, 2001.

Rejections under 35 U.S.C. § 112

Claims 16 and 17 have been rejected under 35 U.S.C. §112 as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. In response to this rejection Applicants amend claim 16 to correct a typographical error consisting of the terms "source" and "drain" being misplaced.

Rejections under 35 U.S.C. § 102(b)

Claims 1 and 16 have been rejected under 35 U.S.C. §102(b) as being anticipated by Middelhoek et al. Applicants submit that Middelhoek et al. does not disclose an apparatus as now recited in independent claims 1 and 16.

Applicants submit that Middelhoek et al. does not disclose a semiconductor device including **"a control gate having...a second portion *formed over a first one of said side walls*** [of said floating gate]**...said second portion *having a***

surface substantially parallel to and opposing said first side wall... as now recited in each of the independent claims 1and 16. Middelhoek et al. teaches utilizing highly doped boundary regions to separate memory cells from one another in order to reduce the lateral spread of depletion layers and prevent parasitic connections between adjacent memory cells, thereby allowing a more dense placement memory cells on a substrate. No embodiment disclosed by Middelhoek et al. discloses a control gate, a portion of which has a surface substantially opposing and parallel to a side wall of a floating gate. The present invention minimizes the size of individual memory cells by minimizing the necessary thickness of insulating layers separating various gates within a memory cell.

Therefore, independent claims 1 and 16 are patentable under 35 U.S.C. §102(b) over Middelhoek et al. Claims 2 and 17 depend from patentable claims 1 and 16 respectively, and as such incorporate all of the limitations of the independent claims rendering them patentable also.

Rejections under 35 U.S.C. § 102(e)

Claims 8 and 10 have been rejected under 35 U.S.C. §102(e) as being anticipated by Chang et al. Applicants assert that Chang et al. does not disclose an apparatus as now recited in independent claim 8.

Applicants submit that Chang et al. does not disclose a semiconductor device wherein **"at least a portion of...said control gate** [is] **disposed over a portion of said substrate and** [is] **separated therefrom by said second insulating layer...wherein a *portion of said control gate is not disposed over said floating gate...*"** as now recited in independent claim 8 of the present application. Chang et al. teaches utilizing the same side wall spacers to define the boundaries of both the floating gate and the control gate, thereby minimizing the poly tunnel oxide thickness. No embodiment disclosed by Chang et al. includes a control gate that is *not* disposed over a floating gate. The present invention minimizes the size of individual memory cells by minimizing the necessary thickness of insulating layers separating various gates within a memory cell.

Therefore, independent claim 8 is patentable under 35 U.S.C. §102(e) over Chang et al. Claim 10 depends from patentable claim 8 and as such incorporate all of the limitations of the independent claim 8 rendering claim 10 patentable also.

Rejections under 35 U.S.C. § 103(a)

Claims 2 and 17 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Middelhoek et al. in view of Chang et al. Claim 9 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Chang et al. in view of Middelhoek et al. Applicants assert that neither Chang et al., nor Middelhoek et al., either individually or collectively disclose an apparatus as now recited in independent claims 1, 8 and 16.

Applicants submit that neither Chang et al., nor Middelhoek et al, either individually or collectively disclose a semiconductor device including **"a control gate having...a second portion *formed over a first one of said side walls*** [of said floating gate]**...said second portion *having a surface substantially parallel to and opposing said first side wall...*"** as now recited in each of the independent claims 1 and 16. Applicants further submit that neither Chang et al., nor Middelhoek et al, either individually or collectively disclose a semiconductor device wherein **"at least a portion of...said control gate** [is] **disposed over a portion of said substrate and** [is] **separated therefrom by said second insulating layer...wherein a *portion of said control gate is not disposed over said floating gate...*"** as now recited in independent claim 8. Chang et al. teaches a method of manufacturing a memory cell in which the boundaries of the control gate are defined by the same spacers used to define the boundaries of the floating gate, precluding the placement of the control gate adjacent to the substrate.

Applicants assert that claims 1, 8 and 16 as now recited, satisfy the requirements of 35 U.S.C. §103(a). MPEP 2143.03 states that: "If an independent claim is nonobvious under 35 U.S.C. §103, then any claim depending therefrom is nonobvious." *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). Independent claims 1, 8 and 16 are patentable under 35 U.S.C. §103(a) over Chang et al. in view of Middelhoek et al. Claims 2, 9 and 17 depend from patentable claims 1, 8 and 16 respectively, and as such incorporate all of the limitations of independent claims 1, 8 and 16 rendering them patentable also.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached pages are captioned "**VERSION WITH MARKINGS TO SHOW CHANGES MADE.**"

Based on the reasons stated above, Applicant believes that claims 1-2, 8-10 and 16-17 are in condition for allowance, and notice thereof is respectfully solicited. Should

a telephone conference be required to expedite the prosecution of this application, the Examiner is respectfully requested to contact the undersigned at the number set out below.

Date: October 18, 2001

Respectfully submitted,

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CERTIFICATE OF MAILING (37 CFR 1.10(a))

CERTIFICATE OF MAILING BY "EXPRESS MAIL" - Rule 10: I hereby certify that this correspondence is being deposited on October 18, 2001 with the U.S. Postal Service "Express Mail Post Office to Addressee" under 37 CFR 1.10 as **Express Mail No. EL745057344US** addressed to: Box RCE, Assistant Commissioner for Patents, Washington, D.C. 20231

Date: October 18, 2001

Yolette Yturralde-Owen

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

1. (Twice Amended) A semiconductor device having at least one transistor, the device comprising:

a substrate having a channel region defined thereon;

a first insulating layer disposed over said channel region and over at least a portion of said substrate;

a floating gate generally disposed over said channel region and separated therefrom by said first insulating layer, said floating gate having at least two side walls and a top surface;

a second insulating layer disposed over said side walls and over said top surface of said floating gate;

a control gate having a first portion disposed over a portion of said substrate and being separated therefrom by said second insulating layer, a second portion formed over a first one of said side walls and a third portion formed over at least a portion of said top surface of said floating gate and being separated from said floating gate by said second insulation layer, [at least a portion of said control gate being disposed over a portion of said substrate and being separated therefrom by said second insulating layer] said second portion having a surface substantially parallel to and opposing said first side wall;

an erase gate formed over a second one of said side walls and over at least a portion of said top surface of said floating gate and being separated from said second one of said side walls by said second insulation layer;

a drain region formed in a portion of said substrate proximate said control gate; and

a source region formed in a portion of said substrate proximate said erase gate.

8. (Once Amended) A memory array disposed on a substrate comprising a plurality of memory cells each having a floating gate separated from said substrate by a first insulating layer, an erase gate, a control gate separated from said floating gate by a second insulating layer, a source region, and a drain region, comprising:

a plurality of rows and columns of interconnected memory cells wherein the control gates of memory cells in the same row are connected by a common word-line, the erase gates of the memory cells in the same rows are connected by a common erase line, the source regions of the memory cells in the same rows are connected by a common source line, and the drain regions of memory cells in the same columns are commonly connected via a common drain line, wherein at least a portion of each said control gate is disposed over a portion of said substrate and separated therefrom by said second insulating layer, and wherein a portion of said control gate is not disposed over said floating gate; and

control circuit connecting to said word-lines, erase lines, source lines and drain lines for operating one or more memory cells of said memory array.

16. (Once Amended) A semiconductor device having at least one transistor, the device comprising:

a substrate having a channel region;

a first insulating layer disposed over said channel region and over at least a portion of said substrate;

a floating gate generally disposed over said channel region and separated therefrom by said first insulating layer, said floating gate having at least two side walls and a top surface;

a second insulating layer disposed over said side walls and over said top surface of said floating gate;

a control gate having a first portion disposed over a portion of said substrate and being separated therefrom by said second insulating layer, a second portion formed over a first one of said side walls and a third portion formed over at least a portion of said top surface of said floating gate and being separated from said floating gate by said second insulation layer, [at least a portion of said control gate being disposed over a portion of said substrate and being separated therefrom by said second insulating layer] said second portion having a surface substantially parallel to and opposing said first side wall;

an erase gate formed over a second one of said side walls and over at least a portion of said top surface of said floating gate and being separated from said second one of said side walls by said second insulation layer;

a source region [drain region] formed in a portion of said substrate proximate said erase gate; and

a drain region [source region] formed in a portion of said substrate proximate said control gate.